REMARKS

Applicant respectfully requests the Examiner to contact the undersigned to conduct an interview before a next action in this application.

Claims 1-47 are pending. Claims 13 and 16-47 are rejected. Claims 1-12, 14, and 15 are withdrawn from consideration.

Claims 13 and 16-47 have been rejected under 35 USC 103(a) as being unpatentable over Belotserkovsky et al. (U.S. Patent No. 6,621,857; hereinafter "Belotserkovsky") in view of Frank et al. (U.S. Patent No. 6,731,622; hereinafter "Frank") and Schuster et al. (U.S. Patent No. 6,591,355; hereinafter "Schuster"). Applicant respectfully traverses this rejection for the reasons set forth below.

Independent claim 13 recites "A time-sliced processor ... comprising: a master control unit including a time slot table and a partial sum table for any time slot granularity; a *data cache* ..." Similarly, independent claim 28 recites "A master control unit in a time-sliced processor ... wherein the master control unit configures and controls the *data cache* and the signal processing elements for any time slot granularity." Similarly, independent claim 37 recites "A time-sliced processor ... comprising ...a master control means ... for configuring and controlling the *data cache* and the signal processing means for any time slot granularity." Thus, each of these independent claims requires a data cache.

Schuster discloses a method for controlling and managing Distributed Shared Memory (DSM). As stated in column 1, lines 24-27, "the DSM is typically implemented as a middleware layer, between the operating system and user applications running on host processors that are linked by a local area network (LAN)." Further, Schuster states in column 1, lines 31-32, that "in order to control access to the shared memory by different applications running on the different hosts, ..." To a person of ordinary skill in the art, Schuster teaches a method of how to access a shared memory by different applications running on different processors (or hosts). The method is not applicable to what is required by the claimed invention for data caching of time-slice based processing. The data

caching at chip or sub-chip resolution is essential to the claimed time-slice based processing which pauses an on-going processing at time slice boundary, switches to some other processing, and resumes the processing later on by reloading the data in cache. Unlike what Schuster's system is designed for, the memory in the claimed apparatus is accessed by a single computing device rather than multiple devices via a local area network (LAN). Therefore, Schuster does not teach or suggest a data caching scheme as claimed.

Belotserkovsky and Frank fail to make up for Schuster's deficiencies.

As asserted in the previous Response, Frank mentions the term "time slot." However, "time slot" in Frank is mentioned in the context of the 3GPP WCDMA standard, which has a specific and different definition than "time slot" as used in the context of the claimed time-sliced processing.

The Examiner responds in the Advisory Action by asserting that this time slot feature in the context of time-sliced processing is not recited in the claims.

Applicant respectfully disagrees. Independent claim 13 is directed to "A *time-sliced processor* ... comprising ... a master control unit including a *time slot* table and a partial sum table for any *time slot* granularity ..." Independent claim 28 is directed to "A master control unit in a *time-sliced processor* ... comprising: a *time slot* table; and ... wherein the master control unit configures and controls the data cache and the signal processing elements for any *time slot* granularity." Independent claim 37 is directed to "A *time-sliced processor* ... comprising: ... a master control means, including a *time slot* table and a partial sum table, for configuring and controlling the data cache and the signal processing means for any *time slot* granularity." Thus, the times slot feature in the context of time-sliced processing is recited in each of the claims.

Independent claims 13, 28, and 37, along with their dependent claims, are patentable over the applied references for at least these reasons. Reconsideration and withdrawal of the prior art rejection is therefore respectfully requested.

In view of the above, Applicant believes the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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